Department Of Computer Application (BCA)
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BCA Sem - 2
Computer Organization and Architecture

Memory Mapped I/O interfaces :-

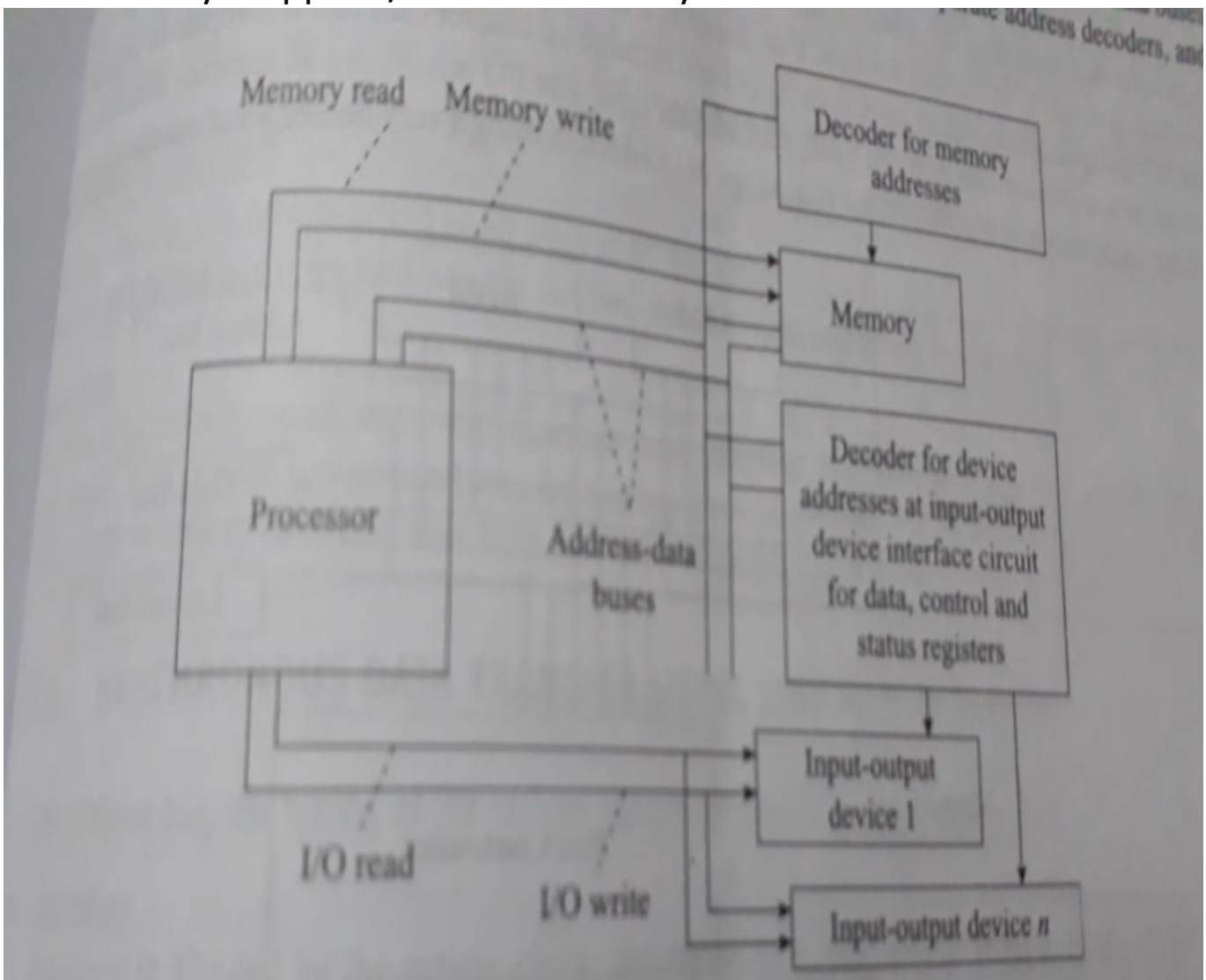
In I/O system, processor must be able to send command to the I/O devices and read data from them. Most of the system use mechanism called memory-mapped I/O. the processor interfaces I/O devices like memory. Processor access to them by common buses,memory and common addressing instruction form memory locations and I/o device register.

As :

1. Control register :- act as a command register and is used to tell the device what the processor want it to do.
2. Status register:- used to tell the processor what the present status of the devices is .
3. Output register or buffer for sending the output through the device.
4. Input register or buffer for receiving the input from the device.

In memory mapped I/O the command register for each I/O device appear to the programmer as memory locations, when the program read and write these memory, hardware transform the memory operation into a transaction over it , in case of read , the result operation is transferred back to the processor over the I/O buses and written into the destination register for the load.

The memory mapped I/O interfaces may be shown as



11.5 I/O Mapped I/O Device Organization on the Distinct Control Bus Signals, wh
Issued when Processing I/O Instructions. The Devices and Memory are Interface
Separate Address Decorders for Memory and for I/O Circuits Accessing Data, Cont

Timing for accessing the I/O bus :-
Time to perform the operations on a bus is the sum of time for a device to request use of the bus, the time to perform arbitration(decide which device can use the bus) and time to complete the operation once a device has been granted access to the bus.
We have two type of buses :-

1. Synchronous data transfer bus
2. Asynchronous data transfer bus.

In the synchronous bus , the timing of the various signals are guided by the master clock.

During input information the timing sequence is

Sequence 1 : guided by master clock, sets the address bits and send an address and command that reaches to slave in time and after setting the bits on the address or command bus
Sequence 2 : master set the command then set the status in time and send to master
Sequence 3 : master reads and receives the slave status bits
Sequence 4: master reads and receives the bits information.

During output :-

Sequence 1 : guided by master clock, the master set the address or command bits that reaches to slave and after setting the bits on the address or command bus.
Sequence 2 : the master sets the command write control signal and sends the write control bit.

Sequence 3: master set the data and send them to the slave after setting the write control bit
Sequence 4: slave write the data bits into its latch which is after receiving the bits from the master.
Sequence5: master deactivate the data bus signals.

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